CLAIM AMENDMENTS

1. (Currently Amended) An apparatus for providing a jittery test signal for use in an integrated circuit (IC) test, the apparatus comprising:

a programmable delay circuit for delaying a first signal with an adjustable delay controlled by an input digital delay word to produce a the jittery test signal for use in the IC, and

first means for supplying a sequence of digital data words as input to the programmable delay circuit for varying the adjustable delay so that the test signal jitters relative to the first signal.

2. (Original) The apparatus in accordance with claim 1 wherein the programmable delay circuit resides within the IC.

3. (Original) The apparatus in accordance with claim 2 wherein the first means comprises a programmable pattern generator.

4. (Currently Amended) The apparatus in accordance with ~~claim 12~~ claim 3 wherein the first means resides within the IC.

5. (Original) The apparatus in accordance with claim 4 wherein the IC includes a subcircuit and wherein the apparatus further comprises:

second means within the IC for selectively applying either the first signal or the test signal as an input signal to the subcircuit.

6. (Currently Amended) The apparatus in accordance with ~~claim 1~~ claim 5 further comprising:

means for delivering the first signal from an input terminal of the IC to the second means.

7. (Original) The apparatus in accordance with claim 5 further comprising:

second means within the IC for selectively applying either a second signal or the test signal as an input signal to the subcircuit.

8. (Original) The apparatus in accordance with claim 7 further comprising:

third means residing within the IC for generating the first signal.

9. (Original) The apparatus in accordance with claim 8 wherein the third means also monitors an output signal of the subcircuit to determine whether it behaves in a particular manner while the second means applies the test signal as the input signal to the subcircuit.

10. (Original) The apparatus in accordance with claim 1

wherein the first means alternatively continuously supplies a digital data word to the programmable delay circuit to hold the adjustable delay constant, and

wherein the apparatus further comprises:

a multiplexer for receiving a second signal and the test signal and for selectively supplying either the second signal or the test signal as the first signal input to the programmable delay circuit, wherein the test signal oscillates when the multiplexer supplies the test signal as the first signal input to the programmable delay circuit with a period that is a function of the delay provided by the programmable delay circuit when the first means continuously supplies a digital data word to the programmable delay circuit to hold the adjustable delay constant.

11. (Original) The apparatus in accordance with claim 10 further comprising:

third means for generating data that is a function of a period of the test signal when the multiplexer supplies the test signal as the first signal input to the programmable delay circuit while the first

means continuously supplies a digital data word to the programmable delay circuit to hold the adjustable delay constant.

12. (Currently Amended) The apparatus in accordance with claim 1 wherein the first means comprises a programmable pattern generator for supplying a sequence of digital delay data words to the programmable delay circuit for varying its delay with time and for alternatively continuously supplying a digital data word to the programmable delay circuit to hold its delay constant,

wherein the IC includes a subcircuit, and

wherein the apparatus further comprises:

second means for selectively applying the test signal as an input signal to the subcircuit; and

a multiplexer for receiving a second signal and the test signal and for supplying the second signal as the first signal input to the programmable delay circuit while the first means is supplying the sequence of digital delay words to the programmable delay circuit and for supplying the test signal as the first signal input to the programmable delay circuit while the first means is ~~g the adjustable delay constant~~ continuously supplying a digital data word to the programmable delay circuit to hold its delay constant,

wherein the test signal oscillates when the multiplexer supplies the test signal as the first signal input to the programmable delay circuit with a period that is a function of the constant delay ~~or~~ of the programmable delay circuit.

13. (Original) The apparatus in accordance with claim 12 wherein the programmable delay circuit, the programmable pattern generator, the second means, and the multiplexer reside within the IC.

14. (Original) The apparatus in accordance with claim 13 further comprising:

third means residing within the IC for generating data that is a function of a period of the test signal when test signal oscillates.

15. (Original) The apparatus in accordance with claim 1 wherein the programmable delay circuit comprises:

a plurality of buffers connected in cascade, each having an output; and

a plurality of capacitive circuit elements, each corresponding to a separate one of the buffers and each providing an adjustable capacitance at an output of its corresponding buffer, wherein the first means controls the delay of the programmable delay circuit by adjusting the adjustable capacitance provided by each of the plurality of capacitive elements.

16. (Original) The apparatus in accordance with claim 15 wherein first means always adjusts the adjustable capacitance of the capacitive circuit elements so that they provide substantially similar amounts of capacitance at the outputs of their corresponding buffers.

17. (Original) The apparatus in accordance with claim 15 wherein first means independently adjusts the adjustable capacitance of each capacitive circuit element.

18. (Original) The apparatus in accordance with claim 15 wherein first means can adjust the adjustable capacitance of at least two of the capacitive circuit elements so that they provide differing amounts of capacitance at the outputs of their corresponding buffers.

19. (Original) The apparatus in accordance with claim 15 wherein each capacitive circuit element comprises:

a plurality of capacitors, and

a plurality of switches controlled by the first means for coupling selected ones of the capacitors to the output of the buffer corresponding to the capacitive circuit element.

20. (Original) The apparatus in accordance with claim 19 wherein each capacitor is provided by an input of a gate having capacitive input impedance.

21. (Original) The apparatus in accordance with claim 15 wherein each capacitive circuit element comprises:

a plurality of gates having inputs linked to the output of the buffer corresponding to the capacitive circuit element, wherein an input capacitance of each gate is a function of a voltage applied to the gate, wherein the first means controls a magnitude of the voltage applied to each gate.

22. (Original) A method for testing a subcircuit of an integrated circuit (IC), the subcircuit having an input for receiving an input signal and an output for producing an output signal, the method comprising the steps of:

a. providing a programmable delay circuit having an adjustable delay controlled by digital delay control data supplied to the programmable delay control circuit;

b. applying a first signal as input to the programmable delay circuit such that the programmable delay circuit delays the first signal to produce a test signal, and

c. supplying a sequence of digital control data to the programmable delay circuit that varies the adjustable delay during step b such that the test signal jitters relative to the first signal.

23. (Original) The method in accordance with claim 22 further comprising the steps of:

d. inverting and applying the test signal as input to the programmable delay circuit and supplying digital delay control data to the programmable delay circuit that holds its adjustable delay constant, such that the test signal oscillates with a period that is a function of the adjustable delay;

e. measuring the period of the test signal;

f. carrying out a plurality of iterations of steps d and e with the adjustable delay held to a different constant value during each iteration.

24. (Currently Amended) The method in accordance with claim 22 further comprising the step of:

g. ascertaining values <u>of</u> digital control data included in the sequence supplied at step c needed to produce a particular jitter pattern in the test signal generated at step c based on the periods of the test signal measured during the plurality of iterations of step c.

25. (Original) The method in accordance with claim 22 wherein step a comprises the forming the programmable delay circuit within the IC.

26. (Original) The method in accordance with claim 25 wherein step c comprises the substeps of:

c1. forming a programmable pattern generator within the IC; and

c2. programming the programmable pattern generator to generate the sequence of digital delay control data.

27. (Original) The method in accordance with claim 25 wherein the programmable delay circuit comprises:

a plurality of cascaded buffers connected in series, each having an output; and

means for applying a capacitance of magnitude controlled by the digital delay control data to the outputs of the buffers.

28. (Original) The method in accordance with claim 27 wherein any change in value of the digital delay control data applied to the programmable delay circuit during step c causes a change in the magnitude of the capacitance applied to the output of each of the cascaded buffers.

29. (Original) The method in accordance with claim 25 further comprising the step of:

d. providing means within the IC for monitoring the output signal of the subcircuit to determine whether the output signal behaves in a particular manner and for sending data from the IC indicating wherein the output signal behaved in that particular manner.

30. (Original) The method on accordance with claim 23 wherein step e comprises counting a number of periods of a periodic reference clock signal occurring during a predetermined number of periods of the test signal.

31. (Original) An apparatus for testing a subcircuit of an integrated circuit (IC), the subcircuit having an input for receiving an input signal and an output for producing an output signal, the apparatus comprising:

a programmable delay circuit residing within the IC for delaying a first clock signal ~~to~~ with a delay selected by a digital delay control word input to the programmable delay circuit to produce a second clock signal;

a programmable pattern generator for providing a sequence of delay control words as input to the programmable delay circuit;

first means for selectively applying the second clock signal as the input signal to the subcircuit;

a multiplexer residing within the IC for receiving a third clock signal and the second clock signal for selectively supplying either the third clock signal or the second clock signal as the first clock signal input to the programmable delay circuit, wherein the second clock signal oscillates when supplied as the first clock signal input to the programmable delay circuit with a period that is a function of the delay provided by the programmable delay circuit; and

a test circuit receiving the second clock signal and for generating a test signal having edges synchronized to edges of the second clock signal.

32. (Original) The apparatus in accordance with claim 31 wherein the programmable delay circuit comprises:

a plurality of buffers connected in series, each having an output; and

second means for adding capacitance of magnitude controlled by each successive digital delay control word of the sequence to outputs of the buffers.

33. (Original) The apparatus in accordance with claim 32 wherein the second means comprises:

a plurality of capacitors, and

a plurality of switches controlled by each successive delay control word of the sequence for selectively coupling the capacitors to inputs of the buffers.

34. (Original) The apparatus in accordance with claim 31 further comprising:

second means residing within the IC for monitoring the output signal of the subcircuit to determine whether it behaves in a particular manner in response to the test signal.

35. (Original) The apparatus in accordance with claim 31 further comprising:

second means for counting a number of periods of a periodic reference clock signal occurring during a predetermined number of periods of the test signal.